Date Mailed: October 22, 2003

Sheet 1 of 1

Form 1449* INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION	Docket Number: G&C 30448.116-US-U1	Application Number: 10/616,021
	Applicants: Jri Lee et al.	
	Filing Date: July 9, 2003	Group Art Unit: 2916

U.S. PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENTS							
	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)		
LW		M. Wurzer et al, "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz f_T Silicon Bipolar Technology," IEEE Journal of Solid-State Circuits, Sept. 1999, 34:1320-1324
LW		M. Reinhold et al, "A Fully Integrated 40-Gb/s Clock and Data Recovery IC with 1:4 DEMUX in SiGe technology," IEEE Journal of Solid-State Circuits, Dec. 2001, 36:1937-1945
LW		J. Cao et al, "OC-192 Receiver in Standard 0.18 μm CMOS," ISSCC Dig. Tech. Papers, Feb. 2002, pp. 250-251
LW		J. Kim and B. Kim, "A Low Phase-Noise CMOS LC Oscillator with a Ring Structure," ISSCC Dig. of Tech. Papers, Feb. 2000, pp. 430-431
LW		T. P. Liu, "A 6.5-GHz Monolithic CMOS Voltage-Controlled Oscillator," ISSCC Dig. of Tech. Papers, Feb. 1999, pp. 404-405
LW		J. E. Rogers and J. R. Long, "A 10-Gb/s CDR/DEMUX with LC Delay Line VCO in 0.18 μm CMOS," ISSCC Dig. of Tech. Papers, Feb. 2002, pp. 254-255
LW		J. Savoj and B. Razavi, "A 10-Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection," ISSCC Dig. Tech. Papers, Feb. 2001, pp. 78-79
LW		M. Danesh et al., "A Q-Factor Enhancement Technique for MMIC Inductors," Proc. IEEE Radio Frequency Integrated Circuits Symp., April 1998, pp. 217–220
LW		A. Hajimiri and T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," IEEE Journal of Solid-State Circuits, Feb. 1998, pp. 179-194
LW		J. D. H. Alexander, "Clock Recovery from Random Binary Data," Electronics Letters, Oct. 1975, 11:541-542
LW		B. Razavi et al, "Design Techniques for Low-Voltage High-Speed Digital Bipolar Circuits," IEEE Journal of Solid-State Circuits, March 1994, pp. 332-9

EXAMINER:	DATE CONSIDERED: 2/16
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form for next communication to the Applicant.	

*Substitute Disclosure Statement Form (PTO-1449)

Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE